



# Table of Contents

<b>1 Introduction</b> .....	<b>1</b>
1.1 Bambino Family of Controllers.....	1
1.2 Bambino 100 Base Features.....	1
1.3 Bambino 100 Optional Features.....	2
<b>2 Hardware</b> .....	<b>3</b>
2.1 Microcontroller.....	3
2.2 ESP12 WiFi Module Option.....	6
2.3 MBED HDK Option.....	6
2.4 Serial Flash Memory Option.....	6
<b>3 User Interfaces, Connectors, and Jumpers</b> .....	<b>7</b>
3.1 Bambino 100 Module Pin Out.....	7
3.2 Onboard Peripherals.....	8

# 1 Introduction

## 1.1 Bambino Family of Controllers

The Micromint Bambino 100 is a multi-core SBC designed for compatibility with microPython or the mbed framework. microPython is an implementation of Python 3 that has been optimized to run on a microcontroller. It allows for quick and easy programs to integrate systems faster. The mbed framework is a popular framework for embedded software development that includes extensive class libraries, tools and broad community support, allowing you to deliver embedded applications faster and more reliably. The Micromint Bambino 100 is powered by an NXP LPC4337, the first dual-core ARM Cortex-M microcontroller. Its Cortex-M4 and Cortex-M0 cores are both capable of concurrent 204 MHz operation. The hardware block diagram and feature summary is included below:

## 1.2 Bambino 100 Base Features

- 204 MHz Dual Core 32-bit ARM® Cortex?-M4/M0
- 1MB of Flash

- 136k of SRAM
- 16k of EEPROM
- 2 USB Device Port
- 2 Push Buttons
- 4 LEDs
- microSD Socket
- 32 GPIO

### **1.3 Bambino 100 Optional Features**

- MBED HDK/CMSIS DAP
  - ESP12 WiFi Module
  - 8M SPIFI Flash
- 

[NEXT: Getting Started](#)

[PREVIOUS: Table of Contents](#)

## 2 Hardware

The following image shows where some of the hardware components are located.

File:Bambino-100-Hardware.png

### Bambino 100 Hardware

## 2.1 Microcontroller

The Bambino 100 includes a NXP LPC4337 microcontroller. These dual core 32-bit ARM Cortex-M4/M0 RISC microcontroller are capable of 204-MHz operation with a Thumb2 instruction set for smaller object code. It uses a Harvard architecture with separate local instruction and data buses as well as a separate peripherals bus. Please see NXP's LPC4337 Microcontroller's User Manual for more information and register definitions.

### 2.1.1 LPC4337 key features

- Cortex-M4 Processor core
  - ◆ ARM Cortex-M4 processor (version r0p1), running at frequencies of up to 204 MHz.
  - ◆ Built-in Memory Protection Unit (MPU) supporting eight regions.
  - ◆ Built-in Nested Vectored Interrupt Controller (NVIC).
  - ◆ Hardware floating-point unit.
  - ◆ Non-maskable Interrupt (NMI) input.
  - ◆ JTAG and Serial Wire Debug (SWD), serial trace, eight breakpoints, and four watch points.
  - ◆ Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
  - ◆ System tick timer.
- Cortex-M0 Processor core
  - ◆ ARM Cortex-M0 co-processor (version r0p0) capable of off-loading the main ARM Cortex-M4 application processor.
  - ◆ Running at frequencies of up to 204 MHz.
  - ◆ JTAG
  - ◆ Built-in NVIC.
- On-chip memory
  - ◆ Up to 1 MB on-chip dual bank flash memory with flash accelerator.
  - ◆ 16 kB on-chip EEPROM data memory.
  - ◆ 136 kB SRAM for code and data use.
  - ◆ Multiple SRAM blocks with separate bus access. Two SRAM blocks can be powered down individually.
  - ◆ 64 kB ROM containing boot code and on-chip software drivers.
  - ◆ 64 bit+ 256 bit of One-Time Programmable (OTP) memory for general-purpose use.
- Configurable digital peripherals
  - ◆ Serial GPIO (SGPIO) interface.
  - ◆ State Configurable Timer (SCTimer/PWM) subsystem on AHB.
  - ◆ Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like the timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces
  - ◆ Quad SPI Flash Interface (SPIFI) with four lanes and up to 52 MB per second.
  - ◆ 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - ◆ One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY.
  - ◆ One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY.
  - ◆ USB interface electrical test software included in ROM USB stack.
  - ◆ One 550 UART with DMA support and full modem interface.
  - ◆ Three 550 USARTs with DMA and synchronous mode support and a smart card interface conforming to ISO7816 specification. One USART with IrDA interface.
  - ◆ Up to two C\_CAN 2.0B controllers with one channel each.
  - ◆ Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - ◆ One SPI controller.
  - ◆ One Fast-mode Plus I2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I2C-bus specification. Supports data rates of up to 1 Mbit/s.
  - ◆ One standard I2C-bus interface with monitor mode and with standard I/O pins.
  - ◆ Two I2S interfaces, each with DMA support and with one input and one output.
- Digital peripherals
  - ◆ External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - ◆ Secure Digital Input Output (SD/MMC) card interface.
  - ◆ Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.

- ◆ Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
- ◆ GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
- ◆ Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- ◆ Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- ◆ Four general-purpose timer/counters with capture and match capabilities.
- ◆ One motor control Pulse Width Modulator (PWM) for three-phase motor control.
- ◆ One Quadrature Encoder Interface (QEI).
- ◆ Repetitive Interrupt timer (RI timer).
- ◆ Windowed watchdog timer (WWDT).
- ◆ Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- ◆ Alarm timer; can be battery powered.
- Analog peripherals
  - ◆ One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - ◆ Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Clock generation unit
  - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - ◆ 12 MHz internal RC oscillator trimmed to 3 % accuracy over temperature and voltage (1.5 % accuracy for Tamb = 0 °C to 85 °C).
  - ◆ Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - ◆ Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL can be used with the High-speed USB, the third PLL can be used as audio PLL.
  - ◆ Clock output.
- Power
  - ◆ Single 3.3 V (2.4 V to 3.6 V) power supply with on-chip DC-to-DC converter for the core supply and the RTC power domain.
  - ◆ RTC power domain can be powered separately by a 3 V battery supply.
  - ◆ Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - ◆ Processor wake-up from Sleep mode via wake-up interrupts from various peripherals. Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
  - ◆ Brownout detect with four separate thresholds for interrupt and forced reset.
  - ◆ Power-On Reset (POR).

### 2.1.2 LPC4337 Block Diagram

### LPC4337 Block Diagram

### 2.1.3 LPC4337 Memory Map

## LPC4337 Memory Map

### 2.2 ESP12 WiFi Module Option

The ESP12 is a WiFi module based on the ESP8266 processor from Espressif. It is a microcontroller with a WiFi front-end and TCP/IP stack with DNS support. The ESP12 can be populated on the bottom of the Bambino 100.

### 2.3 MBED HDK Option

The MBED HDK is powered by NXP's LPC11U35. The mbed HDK uses the CMSIS-DAP Interface design that provides simple USB drag-n-drop programming and CMSIS-DAP debug interface for the target microcontroller.

### 2.4 Serial Flash Memory Option

The Bambino 100 has an optional Quad SPI Flash for program and non-volatile data storage. The quad SPI flash has a maximum clock rate of 80 MHz.

---

[NEXT: User Interfaces, Connectors, and Jumpers](#)

[PREVIOUS: Rebuild Firmware](#)

## 3 User Interfaces, Connectors, and Jumpers

The following image shows where the connectors, headers, and jumpers are located on the Bambino 100.

[File:Bambino-100-Connectors.png](#)

### Bambino 100 User Interfaces, Connectors, and Jumpers

#### 3.1 Bambino 100 Module Pin Out

The Bambino 100's module pin out. The headers use 0.1 inch spacing between pins.

Bambino 100 Module Pin Out							
PIN #	mbed	Arduino	MCU Pin Name	Peripheral	SCU Func	Peripheral	SCU Func
1	GND						
2	VIN						
3	VBAT						
4	RESET						
5	p76	D37	P1_4	GPIO0[11]	0	SSP1_MOSI	5
6	p77	D38	PP1_3	GPIO0[10]	0	SSP1_MISO	5
7	p78	D39	CLK0	CLKOUT	1	SSP1_SCK	6
8	p75	D36	P1_5	GPIO1[8]	0	SSP1_SSEL	5
9	p47	D40	P6_3	GPIO3[2]	0	T2_CAP2	5
10	p48	D41	P6_6	GPIO0[5]	0	T2_CAP3	5
11	p49	D42	P6_7	GPIO5[15]	4	T2_MAT0	5
12	p50	D43	P6_8	GPIO5[16]	4	T2_MAT1	5
13	p68	D27	P4_5	GPIO2[5]	0	CTOUT_5	1
14	p67	D26	P4_2	GPIO2[2]	0	CTOUT_0	1
15	p15	A0	P7_4	GPIO3[12]	0	ADC0_4	8
16	p16	A1	P7_5	GPIO3[13]	0	ADC0_3	8
17	p17	A2	P4_1	GPIO2[1]	0	ADC0_1	7
18	p18	A3	P7_7	GPIO3[15]	0	ADC1_6	8
19	p19	A4	P4_3	GPIO2[3]	0	ADC0_0	8
20	p20	A5	P4_4	GPIO2[4]	0	DAC	8
21	p21	D0	P6_5	GPIO3[4]	0	U0_RXD	2
22	p22	D1	P6_4	GPIO3[3]	0	U0_TXD	2
23	p23	D2	P1_7	GPIO1[0]	0	CTOUT_13	2
24	p24	D3	P4_0	GPIO2[0]	0	NMI	2
25	p25	D4	P6_9	GPIO3[5]	0	T2_MAT2	5

26	p26	D5	P5_5	GPIO2[14]	0	T1_MAT1	5
27	p27	D6	P5_7	GPIO2[7]	0	T1_MAT3	5
28	p28	D7	P7_6	GPIO3[14]	0	CTOUT_11	1
29	p29	D8	P6_12	GPIO2[8]	0	CTOUT_7	1
30	p30	D9	P5_0	GPIO2[9]	0	T1_CAP0	5
31	USB1_DP						
32	USB1_DP						
33	p33	D12	P4_9	GPIO5[13]	4	CTIN_6	1
34	p34	D13	P4_10	GPIO5[14]	4	CTIN2_2	1
35	p35		PE_0	GPIO7[0]	4	CAN1_TD	6
36	p36		PE_1	GPIO7[1]	4	CAN1_RD	6
37	p37	SDA	P2_3	GPIO5[4]	4	I2C1_SDA	1
38	p38	SCL	P2_4	GPIO5[4]	4	I2C1_SCL	1
39	VU						
40	VOUT						

## 3.2 Onboard Peripherals

### 3.2.1 USB0 Device

The Bambino 100 comes equipped with a USB Device Port. The Device port is compliant with the USB V2.0 high-speed device specification. It's connector is a micro USB Type AB.

USB0 Device Port	
Connector Pin#	MCU Pin Name
1	USB0_VBUS (+5.0V)
2	USB0_DM
3	USB0_DP
4	USB0_ID
5	Ground

### 3.2.2 Boot Jumper

The boot jumper is used to put the Bambino 100 into Device Firmware Upgrade (DFU) mode. This is accomplished by shorting the two pins before power is applied or by shorting the pins and pressing the reset button. For further information please see the [Getting Started Section](#) of this manual.

### 3.2.3 User Buttons and LEDs

The Bambino 100 comes standard with a user push button, a reset push button, and four user LEDs. The user push button is connected to GPIO0[7] with a 22k-ohm pull-up resistor connected to it. User LED1 (yellow) can be illuminated by clearing GPIO3[7] of the LPC4337. User LED2 (green) can be illuminated by clearing GPIO5[5]. User LED3 (blue) can be illuminated by clearing GPIO3[0]. User LED4 (red) can be illuminated by clearing GPIO3[1].

User Buttons and LEDs							
BAM100 Peripheral	MCU Pin Name	Peripheral	SCU Func	Peripheral	SCU Func	Peripheral	SCU Func
LED1	P6_11	GPIO3[7]	0	T2_MAT3	5		
LED2	P2_5	GPIO5[5]	4	T3_MAT2	6	USB0_IND0	7
LED3	P6_1	GPIO3[0]	0				
LED4	P6_2	GPIO3[1]	0				
BTN1	P2_7	GPIO0[7]	0				

### 3.2.4 MICRO SD

The microSD socket (J2) enables micro-secure-digital memory cards to be plugged into the Bambino 100 microcontroller board. The microSD card allows the user the ability of a standard removable media for transferring data to and from the Bambino 100. The LPC4337 interfaces to the microSD card through the Secure Digital Input Output card interface.

Micro SD Card		
MCU Pin Name	Peripheral	SCU Func
CLK2	SD_CLK	4
P1_6	SD_CMD	7
P1_9	SD_DAT0	7
P1_10	SD_DAT1	7
P1_11	SD_DAT2	7
P1_12	SD_DAT3	7
P1_13	SD_CD	7

### 3.2.5 ESP12 WiFi (Optional)

The ESP12 WiFi Module adds wireless support to the Bambino 100.

ESP12		
MCU Pin Name	Peripheral	SCU Func
P5_6	U1_TXD	4
P1_14	U1_RXD	1
P5_2	U1_RTS	4
P5_4	U1_CTS	4
P5_1	GPIO2[10]	0

### 3.2.6 MBED HDK/CMSIS DAP (Optional)

The Bambino 100 optionally comes equipped with the MBED HDK. It is powered by NXP's LPC11U35 microcontroller. The MBED HDK is compliant with the USB V2.0 full-speed device specification. It's connector is a micro USB Type AB and is designated J6.

MBED HDK/USB1 Device Port	
Connector Pin#	MBED HDK Pin (LPC11U35)

1	VUSB1
2	USB_DM
3	USB_DP
4	Not Connected
5	Ground

### 3.2.7 MBED HDK/CDC Device (Optional)

The MBED HDK implements a virtual serial port via USB using I/O from UART2 in the LPC4337. This allows simple serial I/O from mbed applications to terminal emulators such as PuTTY.

HDK-CDC		
MCU Pin Name	Peripheral	SCU Func
P2_10	U2_TXD	2
P2_11	U2_RXD	2

### 3.2.8 Serial Flash Memory (Optional)

The Bambino 100 has an option to populate serial flash for program and nonvolatile data storage. It uses the LPC4337's Quad SPI Flash interface (SPIFI). The SPIFI interface has data rates up to 52 MB per second.

Serial Flash Memory		
MCU Pin Name	Peripheral	SCU Func
P3_3	SPIFI_SCK	3
P3_4	SPIFI_SIO3	3
P3_5	SPIFI_SIO2	3
P3_6	SPIFI_MISO	3
P3_7	SPIFI_MOSI	3
P3_8	SPIFI_CS	3

---

[NEXT: Mechanical and Electrical Characteristics](#)

[PREVIOUS: Hardware](#)